University of Bahrain
College of Information technology
Department of Computer Engineering

Test (2)

Student Name	
I.D. No.	
Section	

Course Title: Digital Logic
Course number: ITCE 202
Semester: 2
Academic Year: 2007/2008
Duration : 90 minutes
Date: 8th June 2008

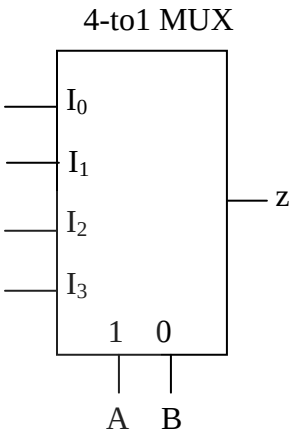
Read the following before you start:
1. Write your name, ID and section number
2. Answer all questions.
3. Write your answers on the attached sheets only.

Question	Mark	Mark attained
1	25	
2	30	
3	15	
4	10	
5	20	
Total	100	

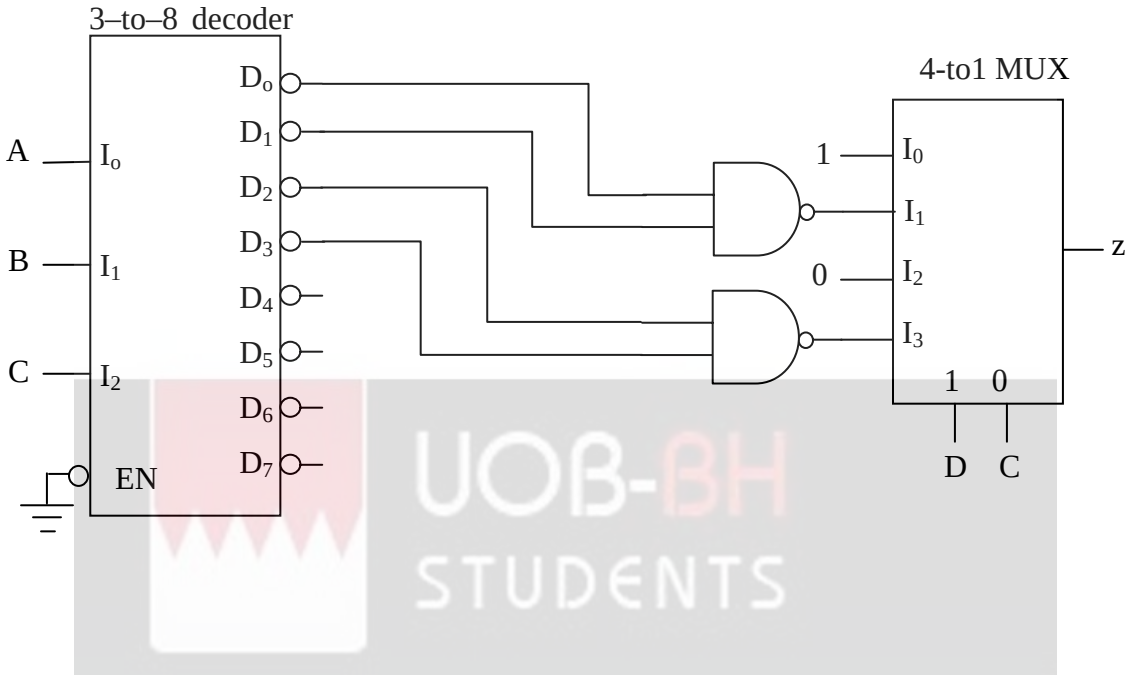
Question [1]: [25 mark]

a. Implement the following Boolean function using 4-to-1 Multiplexer and any additional gates. Use the same notation of the given Multiplexer.

$$f(A,B,C,D) = ACD + B'C'D + B'CD'$$



b. For the circuit shown below, determine the output function z as the minimum sum of products in algebraic form; (give the values of I_1 and I_3 as well).



Question [2] : [30 marks]

a. Derive the next state equation of an T flip-flop.

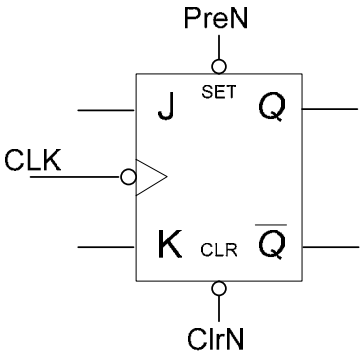
b. Design a binary counter using T Flip-Flops which counts in the sequence:

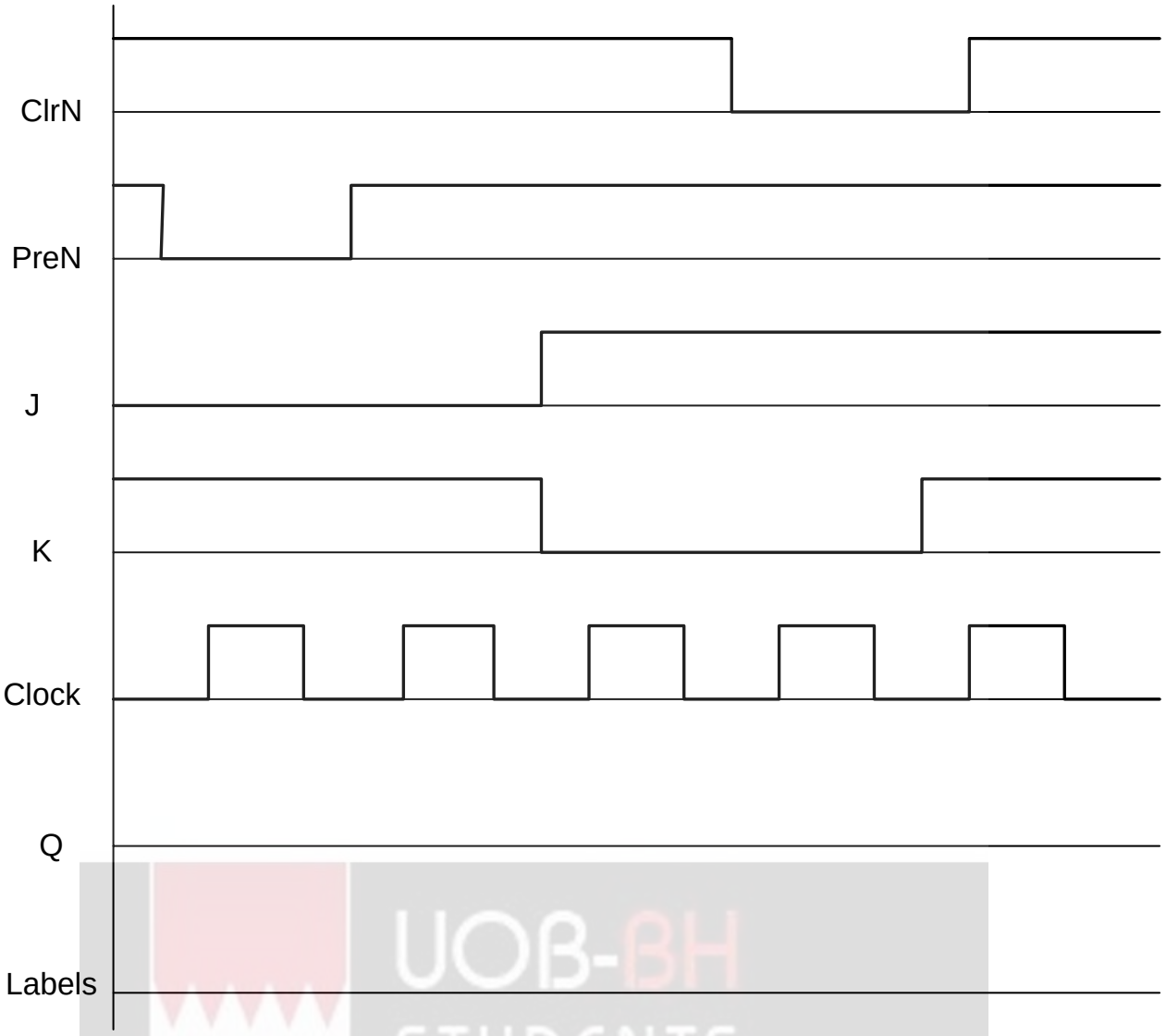
$$0 \rightarrow 3 \rightarrow 5 \rightarrow 7 \rightarrow 2 \rightarrow 6$$ and repeat

c. Draw a complete state diagram for the counter in part b showing what happens when the counter is started in each unused states.

Question [3] : [15 marks]

Complete the following timing diagram for a J-K flip-flop shown in the figure. Label the different states of Q as one of the following (Set, Reset, PreN, ClrN, no Q change, Q change). Assume initial value Q=0.





Question [4]: [10 marks]
Explain how to convert a single J-K-flip flop to T-flip flop. Show all of your steps. Draw the converted J-K flip flop with any additional gates.

Question [5]: [20 marks]

For the register shown below, complete the table which describes the operation of the circuit. The register will change state after each clock pulse. The clock pulses are applied one after the other and the next state will depend on the previous state values. Fixed values are applied to DC_{in}, DB_{in} and DA_{in}, which are 011 respectively. Ct control signal is a count signal where the register contents will increment.

	ClrN	Ld	Ct	C+	B+	A+	Action
1st clk	0	0	0				
2nd	1	1	1				
3rd	1	0	1				
4th	1	0	0				
5th	1	0	1